WHAT IS CLAIMED IS:

1. A microelectronic device, comprising:

an insulator located over a substrate;

a semiconductor feature located over the insulator and having a thickness, a first surface opposite the insulator, and a sidewall spanning at least a portion of the thickness; and

a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall.

2. The device of claim 1 wherein a portion of the semiconductor feature interposes the insulator and the second member of the contact layer.

3. The device of claim 2 wherein the portion of the semiconductor feature interposing the insulator and the second member of the contact layer has a thickness of at least about 50 Angstroms.

4. The device of claim 2 wherein the portion of the semiconductor feature interposing the insulator and the second member of the contact layer has a thickness of less than about 100 Angstroms.

5. The device of claim 1 wherein the contact layer comprises a third member connected to the second member and interposing a portion of the insulator and a portion of the semiconductor feature.

6. The device of claim 5 wherein the third member of the contact layer has a thickness of at least about 10 Angstroms.

7. The device of claim 1 wherein the contact layer comprises metal.

8. The device of claim 1 wherein the contact layer comprises metal silicide.

9. The device of claim 1 wherein the contact layer comprises cobalt silicide.

10. The device of claim 1 wherein the contact layer comprises nickel silicide.

11. The device of claim 1 wherein the contact layer comprises metal nitride.

12. The device of claim 1 wherein the contact layer comprises metal oxide.

13. The device of claim 1 wherein the first member of the contact layer has a thickness of less than about 400 Angstroms.

14. The device of claim 1 wherein the semiconductor feature comprises silicon.

15. The device of claim 1 wherein the semiconductor feature comprises silicon and germanium.

16. The device of claim 1 wherein the semiconductor feature comprises silicon and carbon.

17. The device of claim 1 wherein the semiconductor feature comprises silicon, germanium and carbon.

18. The device of claim 1 wherein the semiconductor feature has a thickness of at least about 400 Angstroms.

19. The device of claim 1 wherein the semiconductor feature has a thickness of at least about 100 Angstroms.

20. The device of claim 1 wherein the insulator comprises an oxide.

21. The device of claim 1 wherein the insulator comprises silicon nitride.

22. The device of claim 1 wherein the insulator comprises silicon oxynitride.

23. The device of claim 1 wherein the insulator comprises a high-k dielectric material.

24. The device of claim 1 wherein the insulator comprises a buried oxide layer.

25. The device of claim 1 wherein the substrate is a silicon-on-insulator (SOI) substrate having an insulating layer interposing a semiconductor layer and a bulk substrate, the insulator is defined in the insulating layer, and the semiconductor feature is defined in the semiconductor layer.

26. A transistor device, comprising:

an insulator located over a substrate;

a gate located over the insulator;

source and drain regions on opposing sides of the gate and having a thickness over the insulator, each of the source and drain regions having a first surface opposite the insulator and a sidewall distal from the gate and spanning at least a portion of the thickness; and

source and drain contacts each having a first member extending over at least a portion of a corresponding first surface and a second member spanning at least a portion of a corresponding sidewall.

27. The device of claim 26 wherein a portion of at least one of the source and drain regions interposes the insulator and the second member of a corresponding one of the source and drain contacts.

28. The device of claim 26 wherein the interposing portion has a thickness of at least about 50 Angstroms.

29. The device of claim 26 wherein the interposing portion has a thickness of less about than 100 Angstroms.

30. The device of claim 26 wherein at least one of the source and drain contacts includes a third member connected to a corresponding second member and interposing a portion of the insulator and a portion of a corresponding one of the source and drain regions

31. The device of claim 26 wherein the third member has a thickness of at least about 10 Angstroms.

32. The device of claim 26 wherein at least one of the source and drain contacts comprises metal.

33. The device of claim 26 wherein at least one of the source and drain contacts comprises metal silicide.

34. The device of claim 26 wherein the contact layer comprises cobalt silicide.

35. The device of claim 26 wherein the contact layer comprises nickel silicide.

36. The device of claim 26 wherein at least one of the source and drain contacts comprises metal nitride.

37. The device of claim 26 wherein at least one of the source and drain contacts comprises metal oxide.

38. The device of claim 26 wherein the first member of at least one of the source and drain contacts has a thickness of less than about 400 Angstroms.

39. The device of claim 26 wherein at least one of the source and drain regions comprises silicon.

40. The device of claim 26 wherein at least one of the source and drain regions comprises silicon and germanium.

41. The device of claim 26 wherein at least one of the source and drain regions comprises silicon and carbon.

42. The device of claim 26 wherein at least one of the source and drain regions comprises silicon, germanium and carbon

43. The device of claim 26 wherein at least one of the source and drain regions has a thickness of at least about 400 Angstroms.

44. The device of claim 26 wherein at least one of the source and drain regions has a thickness of at least about 100 Angstroms.

45. The device of claim 26 wherein the insulator comprises an oxide.

46. The device of claim 26 wherein the insulator comprises silicon nitride.

47. The device of claim 26 wherein the insulator comprises silicon oxynitride.

49. The device of claim 26 wherein the insulator comprises a high-k dielectric material.

50. The device of claim 26 wherein the insulator is comprise a buried oxide layer.

51. A method of manufacturing a microelectronic device, comprising:

forming an insulator over a substrate;

forming a semiconductor feature having a thickness over the insulator, a first surface opposite the insulator and a sidewall spanning at least a portion of the thickness; and

forming a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall.

52. The method of claim 51 wherein a portion of the semiconductor feature interposes the insulator and the second member of the contact layer.

53. The method of claim 51 wherein the portion of the semiconductor feature interposing the insulator and the second member of the contact layer has a thickness of at least about 50 Angstroms.

54. The method of claim 51 wherein the portion of the semiconductor feature interposing the insulator and the second member of the contact layer has a thickness of less than about 100 Angstroms.

55. The method of claim 51 wherein the contact layer includes a third member connected to the second member and interposing a portion of the insulator and a portion of the semiconductor feature.

56. The method of claim 51 wherein the third member of the contact layer has a thickness of at least about 10 Angstroms.

57. An integrated circuit device, comprising:

an insulator located over a substrate;

a plurality of microelectronic devices each including:

a semiconductor feature having a thickness over the insulator, a first surface opposite the insulator and a sidewall spanning at least a portion of the thickness; and

a contact layer having a first member extending over at least a portion of the first surface and a second member spanning at least a portion of the sidewall;

a plurality of dielectric layers located over the plurality of microelectronic devices; and

a plurality of interconnects extending through ones of the plurality of dielectric layers, at least one of the plurality interconnects interconnecting ones of the plurality of microelectronic devices.

58. The integrated circuit device of claim 57 wherein a portion of each of the semiconductor features interposes the insulator and the second member of a corresponding contact layer.

59. The integrated circuit device of claim 57 wherein ones of the contact layers include comprise a third member connected to a corresponding second member and interposing a portion of the insulator and a portion of a corresponding semiconductor feature.